ABSTRACT OF THE DISCLOSURE

What is disclosed is: a semiconductor integrated circuit comprising; a first controlling circuit section, a level transforming circuit, a first buffer circuit, a second buffer circuit, an overvoltage protecting circuit; wherein a first n-channel type MOS transistor is provided in the first buffer circuit and a second p-channel type MOS transistor is provided in the second buffer circuit. Thus, faster operation can be obtained. And, voltage between source and drain of a third p-channel type MOS transistor and a third n-channel type MOS transistor of the overvoltage protecting circuit, impressed when output signal OUT changes, can be decreased.